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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/348,885	07/01/1999	DAVID C. TANNENBAUM	15-4-849.00	5888

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EXAMINER	
NGUYEN, PHU K	

ART UNIT	PAPER NUMBER
2671	24

DATE MAILED: 04/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/348,885	TANNENBAUM, DAVID C.	
	Examiner	Art Unit	
	Phu K. Nguyen	2671	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

PHU K. NGUYEN
PRIMARY EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over GULLEY et al. (5,025,407) in view of EL-NAGGAR et al. (5,061,866).

As per claim 1, Gulley teaches the claimed "dual mode device for generating a cross product or a dot product from a first vector and a second vector, the first vector having a first set of components and the second vector having a second set of components" (Gulley, figure 12, register banks 1203 and 1204; column 18, lines 52-63), the device comprising: "a dual mode controller receiving the first and second vectors, the dual mode controller being configured to select vector components for evaluating a cross product component or a dot product in response to a first signal, the first signal indicting whether to generate a cross product component or a dot product" (Gulley, column 19, lines 1-13); and "a dual mode unit coupled to receive the selected vector components for generating the gross product component or the dot product in response to the first signal" (Gulley, FPU 1206). It is noted that Gulley does not explicitly teach that the dual mode unit "comprising a plurality of shared logic units that are used to generate the cross product component and the dot product". However, El-Naggar teaches that such "dual mode unit comprising a plurality of shared logic units that are used to generate the cross product component and the dot product" is well known in the art (El-Naggar, figure 7; column 2, lines 15-20). Thus, it would have been obvious to a

person of ordinary skill in the art at the time the invention was made, in view of the teaching of El-Naggar, to configure Gulley's system as claimed by sharing the multiplier/summer to generate the scalar of the dot product or the components of the cross-product vector because such sharing the common multiplier/adder will reduce the hardware required for process.

Claim 2 adds into claim 1"the dual mode unit outputs the cross product component when the first signal indicates generation of the cross product component and wherein the dual mode unit outputs the dot product when the first signal indicates generation of the dot product" which Gulley teaches in column 19, lines 2-13.

Claim 3 adds into claim 1"the dual mode controller receives a second signal for indicating the cross product component to be generated and selects the vector components for evaluating the cross product component in response to the second signal" which Gulley teaches in column 18, lines 56-68.

Claim 4 adds into claim 1"the dual mode controller selects the vector components that are different from the cross product component to be generated when the first signal indicates generation of the cross product component" which would have been obvious because the computer instructions need proper vector components to perform multiplier/adder for sufficiently generate the cross product.

Claim 5 adds into claim 1"the dual mode controller changes the sign of one or more selected vector components for transmission to the dual mode unit when the first signal indicates generation of the cross product component" which would have been obvious because the computer instructions need proper operations to perform multiplier/adder for sufficiently generate the cross product vector's components.

Claim 6 adds into claim 1"the first set of components includes Ax, Ay, and Az and the second set of components includes Bx, By, and Bz, and wherein the dual mode controller selects all components of the first and second sets when the first signal indicates generation of the dot product" which Gulley teaches in column 19, lines 2-13.

Claim 7 adds into claim 1"the dual mode unit includes a plurality of multipliers and adders that are arranged to generate the cross product component or the dot product" which Gulley teaches in column 19, lines 2-13.

Claim 8 adds into claim 7 "the dual mode unit uses at least one multiplier and at least one adder to generate the cross product component or the dot product" which would have been obvious because the components of the cross product vector are needed at least a multiplier/adder to generate.

Claim 9 adds into claim 1 "the dual mode controller is configured to select the vector components for evaluating the cross product when the first signal indicates

generation of the cross product, wherein the dual mode unit includes a plurality of sub-dual mode units for generating a plurality of cross product vector components, each sub-dual mode unit generating one cross product vector component such that the dual mode unit generates a cross product of the first and second vectors" which would have been obvious because there are a plurality of components for a cross product vector in which each component can be generated from a sub-dual mode unit.

Claim 10 adds into claim 1 "the dual mode unit is used in a lighting subsystem that is configured to generate diffuse light, specular light, or spotlight values" which would be obvious because the generating of shading image using Phong model requires both cross product vector and dot product from the vectors of lights and viewing direction.

As per claim 11, Gulley teaches the claimed "dual mode device for generating a cross product or a dot product from a first vector and a second vector, the first and second vectors having a plurality of components" (Gulley, figure 12, register banks 1203 and 1204; column 18, lines 52-63), the device comprising: "a dual mode controller receiving the first and second vectors, the dual mode controller being configured to select vector components for evaluating a cross product or a dot product in response to a first signal, the first signal indicating whether to generate a cross product or a dot product" (Gulley, column 19, lines 1-13); and " a plurality of dual mode units coupled to receive the selected vector components for generating the cross product or the doc

product in response to the first signal, each dual mode unit generating one cross product vector component of the cross product, the dual mode units generating and outputting the cross product vector components as the cross product when the select signal indicates generation of the cross product component" which would have been obvious because there are a plurality of components for a cross product vector in which each component can be generated from a sub-dual mode unit. It is noted that Gulley does not explicitly teach that the dual mode unit "comprising a plurality of shared logic units that are used to generate the cross product component and the dot product". However, El-Naggar teaches that such "dual mode unit comprising a plurality of shared logic units that are used to generate the cross product component and the dot product" is well known in the art (El-Naggar, figure 7; column 2, lines 15-20). Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made, in view of the teaching of El-Naggar, to configure Gulley's system as claimed by sharing the multiplier/summer to generate the scalar of the dot product or the components of the cross-product vector because such sharing the common multiplier/adder will reduce the hardware required for process.

Claim 12 adds into claim 11 " the dual mode controller changes the sign of one or more selected vector components for transmission to the dual mode units when the first signal indicates generation of the cross product" which would have been obvious because the computer instructions need proper operations to perform multiplier/adder for sufficiently generate the cross product vector's components.

Claim 13 adds into claim 11 " the first vector includes components Ax, Ay, and Az and the second includes components Bx, By, and Bz such that the dual mode units generate the cross product by producing cross product components Cx, Cy, and Cz" which Gulley teaches in column 19, lines 2-13.

Claim 14 adds into claim 12 "one of the dual mode units is selected to generate the dot product of the first and second vectors when the first signal indicates generation of the dot product" which Gulley teaches in column 19, lines 2-13.

Claim 15 adds into claim 11 "wherein the dual mode units are used in a lighting subsystem that is configured to generate a diffuse light value, a specular light value, and a spotlight value" which would be obvious because the generating of shading image using Phong model requires both cross product vector and dot product from the vectors of lights and viewing direction.

Claim 16 adds into claim 11 " the dual mode unit uses at least one multiplier and at least one adder to generate the cross product component or the dot product" which would have been obvious because the components of the cross product vector or the dot product are needed at least a multiplier/adder to generate.

Claim 17 adds into claim 16 " wherein the dual mode unit uses at least one multiplier and at least one adder to generate the cross product component or the dot product" which would have been obvious because the components of the cross product vector or the dot product are needed at least a multiplier/adder to generate.

As per claim 18, Gulley teaches the claimed "computer system having a graphics subsystem comprising a dual mode device, the dual mode device comprising a dual mode controller and a dual mode unit, a method for generating a cross product or a dot product from a first vector and a second vector, the first vector having a first set of components and the second vector having a second set of components" (Gulley, figure 12, register banks 1203 and 1204; column 18, lines 52-63), the method comprising: "receiving the first and second vectors for generating a cross product component or a dot product at the dual mode controller; receiving the first signal indicating whether to generate a cross product component or a dot product at the dual mode controller; selecting vector components for evaluating the cross product component or the dot product in response to the first signal; sending the selected vector components to the dual mode unit" (Gulley, column 19, lines 1-13); and "in response to the first signal and the selected vector components, generating the cross product component when the first signal indicates generation of the dot product" (Gulley, FPU 1206). It is noted that Gulley does not explicitly teach that the dual mode unit "comprising a plurality of shared logic units that are used to generate the cross product component and the dot product".

However, El-Naggar teaches that such "dual mode unit comprising a plurality of shared logic units that are used to generate the cross product component and the dot product" is well known in the art (El-Naggar, figure 7; column 2, lines 15-20). Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made, in view of the teaching of El-Naggar, to configure Gulley's system as claimed by sharing the multiplier/summer to generate the scalar of the dot product or the components of the cross-product vector because such sharing the common multiplier/adder will reduce the hardware required for process.

Claim 19 adds into claim 18 " wherein the sign of one or more selected vector components are changed for evaluating the cross product component when the first signal indicates generation of the cross product component" which would have been obvious because the computer instructions need proper operations to perform multiplier/adder for sufficiently generate the cross product vector's components.

Claim 20 adds into claim 18 "wherein a plurality of cross product vector components comprising a cross product vector are generated in parallel" which would have been obvious because these components can be separately calculated and the parallel operation helps improve the speed of calculation.

Due to new ground of the rejection cited above, this action has been made NON-FINAL.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phu K. Nguyen whose telephone number is (703)305 - 9796. The examiner can normally be reached on M-F 8:00-4:30.

The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Phu K. Nguyen
April 19, 2004